

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An electronic device for generating a clock signal for an integrated circuit, the device comprising:

at least two oscillators configured to generate a single clock signal at a clock output in response to an input signal and to operate in a mutually exclusive manner, the outputs of said oscillators being selectively connectable to said clock output;

means for receiving a data pattern representative of a sequence of two or more frequencies at which said clock signal is required to be generated;

means for causing an oscillator other than the oscillator generating the clock signal at the immediately previous frequency in said sequence to generate a clock signal at a next frequency in said sequence;

means for causing the clock signal at the immediately previous frequency in said sequence to be disconnected from said clock output; and

means for causing the clock signal at the next frequency in said sequence to be connected to said clock output;

wherein the oscillator being caused to generate a clock signal at each frequency in said sequence is independent of the value of said each frequency.

2. (previously presented) The electronic device as recited in claim 1, wherein the clock signal at the immediately previous frequency in said sequence is caused to be disconnected from said clock output prior to connection of the clock signal at the next frequency in the sequence to said clock output.

3. (previously presented) The electronic device as recited in claim 1, wherein generation

of the clock signal at said next frequency in said sequence is commenced prior to disconnection of the clock signal at the immediately previous frequency in the sequence from the clock output.

4. (previously presented) The electronic device as recited in claim 1, wherein connection of the clock signal at the next frequency in said sequence to said clock output is caused to occur when said clock signal is low.

5. (previously presented) The electronic device as recited in claim 1, wherein disconnection of the clock signal at said immediately previous frequency in said sequence from said clock output is caused to occur when said clock signal is low.

6. (previously presented) The electronic device as recited in claim 1, wherein said at least two oscillators comprise programmable ring oscillators.

7. (previously presented) The electronic device as recited in claim 6, comprising a variable programmable delay element for receiving data representative of the duration of a clock cycle of each frequency in said sequence.

8. (previously presented) The electronic device as recited in claim 7, wherein said variable programmable delay element causes the respective oscillator to generate a clock signal at the required frequency.

9. (previously presented) The electronic device as recited in claim 1, wherein said data pattern is derived from, or comprises, a series of requests for a change of frequency of said clock signal.

10. (previously presented) The electronic device as recited in claim 9, further comprising an arbiter for determining the order in which said requests are to be effected.

11. (previously presented) An electronic device according to claim 10, wherein said

arbitrator orders said requests for action on a first-in-first-out basis.

12. (previously presented) The electronic device as recited in claim 11, wherein if two requests are received at substantially the same time, the arbitrator is arranged to randomly select the order in which action is taken on these two requests.

13. (previously presented) The electronic device as recited in claim 1, further comprising an event controller for controlling the order in which said oscillators are caused to commence and cease generating a clock signal and/or the order in which said clock signals are connected and disconnected from said clock output.

14. (previously presented) The electronic device as recited in claim 9, arranged and configured to temporarily disconnect all of the oscillators from the clock output, in response to a request to do so.

15. (currently amended) A method of generating a clock signal for an integrated circuit, the method comprising:

- providing at least two oscillators arranged and configured to generate a single clock signal at a clock output in response to an input signal and to operate in a mutually exclusive manner, the outputs of said oscillators being selectively connectable to said clock output;

- receiving a data pattern representative of a sequence of two or more frequencies at which said clock signal is required to be generated;

- receiving data representative of the next frequency in said sequence;

- causing an oscillator other than the oscillator generating the clock signal at the immediately previous frequency in said sequence to generate a clock signal at said next frequency;

- causing the clock signal at the immediately previous frequency in said sequence to be disconnected from said clock output; and

- causing the clock signal at the next frequency in said sequence to be connected to said clock output;

wherein the oscillator being caused to generate a clock signal at each frequency in said sequence is independent of the value of said each frequency.

16-18. (canceled)